1. A method comprising:

determining whether a supply voltage reaches a predetermined level;

generating pulses to indicate that a supply voltage is ramping up;

terminating the generation of said pulses after said supply voltage reaches a predetermined level; and

preventing the pulses from being generated until after the next power cycle.

2. The method of claim 1 including resetting said logic to its predetermined initial state in response to said pulse.

3. The method of claim 2 including indicating when said supply voltage has reached its predetermined level and providing a signal to a latch in response thereto.

4. The method of claim 3 including determining whether said logic is in its predetermined initial state and if so, providing a signal to said latch.

5. The method of claim 4 including stopping the generation of a signal to reset said logic to its initial state after said logic has provided a signal to said latch indicating that the logic is in its predetermined initial

state and the supply voltage has reached its predetermined level.

6. The method of claim 5 including preventing said latch from thereafter changing state until the power supply cycles again.

7. The method of claim 1 including determining when the pulses are no longer generated.

8. The method of claim 7 including preventing the generation of said pulses after the pulses are no longer generated and prior to a power cycle.

9. The method of claim 1 including emulating logic that is difficult to trigger and determining whether the power supply voltage has reached a level sufficient to trigger the difficult to trigger logic.

10. The method of claim 9 wherein determining whether a supply voltage reaches a predetermined level includes determining whether a voltage is above at least two transistor threshold voltages.

11. An integrated circuit comprising:

an activation circuit to determine whether a supply voltage reaches a predetermined level;

a pulse generator to generate pulses to indicate that a supply voltage is ramping up and to terminate the generation of the pulses after the supply voltage reaches a predetermined level; and

said activation circuit to prevent the pulses from being generated again, after the generation of the pulses has been terminated, until after the next power cycle.

12. The integrated circuit of claim 11 further including a logic functionality to emulate logic that is difficult to trigger and to determine whether the supply voltage has reached a level sufficient to trigger the difficult to trigger logic.

13. The integrated circuit of claim 11 including a level detector that detects when a voltage is above at least two transistor threshold voltages, said level detector operative to control said pulse generator.

14. The integrated circuit of claim 11 including a feedback path that provides the output of said pulse generator to said activation circuit.

15. The integrated circuit of claim 14 including an inverter that creates a high signal in response to a low signal on said feedback path.

16. The integrated circuit of claim 15 including a pair of transistors that must both conduct in order to generate said pulses.

17. The integrated circuit of claim 16 including a capacitor circuit to enable the supply voltage to reach a designated output level.

18. The integrated circuit of claim 17 including a hysteresis sense stage coupled to said capacitor circuit.

19. The integrated circuit of claim 11 wherein said activation circuit includes an inverter coupled to the gate of a load transistor, a second transistor coupled to said load transistor and a third transistor coupled between said load transistor and said first transistor.

20. The integrated circuit of claim 11 including a circuit to latch the pulse generator in response to the supply voltage being in a first state.

21. A power-on reset pulse generator comprising:

a first circuit to develop a pulse indicating that a power supply voltage is not in a first state; and

a second circuit coupled to said first circuit to latch the first circuit in response to the power supply voltage being in the first state.

22. The generator of claim 21 wherein said second circuit latches the first circuit until the next power cycle.

23. The generator of claim 21 including a logic functionality that emulates logic that is difficult to trigger.

24. The generator of claim 23 wherein said logic functionality is coupled to the supply voltage.

25. The generator of claim 21 wherein said second circuit includes a level detector that detects when a voltage is above at least two transistor threshold voltages, said level detector operative to control said first circuit.

26. The generator of claim 21 including a feedback path from the output of said first circuit to said second circuit.

27. The generator of claim 26 including an inverter coupled in said feedback path.

28. The generator of claim 27 including a pair of transistors that must both conduct in order to generate said pulse.

29. The generator of claim 28 including a capacitor circuit to enable the supply voltage to reach a designated output level.

30. The generator of claim 29 including a hysteresis sense stage coupled to said capacitor circuit.